

I claim:

- 2/13/1
1. A buried fuse reading device, comprising:
    - at least one buried fuse;
    - at least one sense amplifier sensing a condition of the buried fuse; and
    - a validation circuit detecting and indicating when output from the sense amplifier is valid.
  2. The device of claim 1, wherein the validation circuit detects when the sense amplifier has sufficiently settled on a sensed condition of the buried fuse.
  3. The device of claim 2, further comprising:
    - a power control circuit for powering the buried fuse reading device up and down; and wherein
    - the validation circuit detects when the sense amplifier has sufficiently settled on a sensed condition once the power control circuit begins powering up the buried fuse reading device.
  4. The device of claim 3, further comprising:
    - a bias generating circuit for generating first and second voltages; and
    - wherein
    - the sense amplifier operates based on the first and second voltages.
  5. The device of claim 4, wherein the validation circuit operates based on the first and second voltages.
  6. The device of claim 5, wherein

the sense amplifier includes a first PMOS transistor and a first NMOS transistor connected in series with the buried fuse, a gate of the first PMOS transistor receiving the first voltage and a gate of the first NMOS transistor receiving the second voltage; and

the validation circuit includes a second PMOS transistor and a second NMOS transistor connected in series, a gate of the second PMOS transistor receiving the first voltage and a gate of the second NMOS transistor receiving the second voltage, the second PMOS and NMOS transistor being weaker than the first PMOS and NMOS transistor, respectively.

7. The device of claim 1, comprising:

- a plurality of buried fuses; and
- a sense amplifier associated with each of the buried fuses.

8. A buried fuse reading device, comprising:

- at least one buried fuse;
- at least one sense amplifier sensing a condition of the buried fuse; and
- a validation circuit dynamically adjusting a validation point of the sense amplifier based on operating conditions, the validation point being a point in time when output from the sense amplifier is considered valid.

9. The device of claim 8, further comprising:

- a power control circuit for powering the buried fuse reading device up and down; and wherein

the validation point is the point in time when output from the sense amplifier is considered valid once the power control circuit begins powering up the buried fuse reading device.

10. The device of claim 9, further comprising:

a bias generating circuit for generating first and second voltages; and  
wherein

the sense amplifier operates based on the first and second voltages.

11. The device of claim 10, wherein the validation circuit operates based on the first and second voltages.

12. The device of claim 11, wherein

the sense amplifier includes a first PMOS transistor and a first NMOS transistor connected in series with the buried metal fuse, a gate of the first PMOS transistor receiving the first voltage and a gate of the first NMOS transistor receiving the second voltage; and

the validation circuit includes a second PMOS transistor and a second NMOS transistor connected in series, a gate of the second PMOS transistor receiving the first voltage and a gate of the second NMOS transistor receiving the second voltage, the second PMOS and NMOS transistor being weaker than the first PMOS and NMOS transistor, respectively.

13. The device of claim 8, comprising:

a plurality of buried fuses; and

a sense amplifier associated with each of the buried fuses.

14. A buried fuse reading device, comprising:

at least one buried fuse;

at least one sense amplifier sensing a condition of the buried fuse; and

a tracking circuit tracking operation of the sense amplifier such that the tracking circuit indicates when the sense amplifier has sufficiently settled on a sensed condition of the buried fuse.

15. The device of claim 14, comprising:  
a power control circuit;  
and down

16. The device of claim 15,  
circuit draw substantially no  
buried fuse reading device po

15. The device of claim 14, comprising:  
a power control circuit;  
and down

16. The device of claim 15,  
circuit draw substantially no  
buried fuse reading device po

15. The device of claim 14, comprising:  
a power control circuit;  
and down

16. The device of claim 15,  
circuit draw substantially no  
buried fuse reading device po

15. The device of claim 14, comprising:  
a power control circuit;  
and down

16. The device of claim 15,  
circuit draw substantially no  
buried fuse reading device po